In the Claims:

Claims **1 to 17** (canceled).

18. (new) A circuit arrangement that can be externally tested through an output pin, comprising an integrated circuit that comprises:

a signal output pin;

a circuit unit;

a control unit having a testing input connected to said signal output pin for testing a potential at said signal output pin, and having a control output providing a control signal responsive to the testing of the potential; and

a switching element having a signal input connected to an output of said circuit unit, a switched signal output connected to said signal output pin, and a control input connected to said control output of said control unit.

19. (new) The circuit arrangement according to claim 18, wherein said control unit comprises:

an amplifier interposed between said output of said circuit unit and said signal input of said switching element, for amplifying, relative to the potential at said signal output pin, a signal provided from said output of said circuit unit via said amplifier and said switching element to said signal output pin;

at least two comparators with inputs connected to said testing input of said control unit and forming a voltage

window discriminator for comparatively testing the potential at said signal output pin; and

a logic gate having at least one input connected to and for performing a logic operation on outputs of said comparators and another output of said circuit unit, and having an output connected to said control output of said control unit, which is connected to said control input of said switching element and which is further connected to said circuit unit for selection of respective circuit elements within said circuit unit.

20. (new) The circuit arrangement according to claim 18, further comprising at least one resistor connected to a reference voltage externally from said integrated circuit, and a switch arrangement interposed between said at least one resistor and said signal output pin of said integrated circuit for selectively connecting said signal output pin through a selected resistor among said at least one resistor to said reference voltage for establishing said potential at said signal output pin.

21. (new) A method of testing an integrated circuit comprising the steps:

a) providing at least one output signal generated by a circuit unit of said integrated circuit to at least one signal output pin of said integrated circuit during a normal operating mode;

b) externally applying an externally applied potential to at least one selected output pin among said at least one signal output pin;

c) evaluating a potential value of said externally applied potential;

d) dependent on and responsive to a result of said evaluating, switching from said normal operating mode into a test mode; and

e) during said test mode, generating in said circuit unit at least one test signal that is to be tested, and proving said at least one test signal to at least one chosen output pin among said at least one signal output pin.

22. (new) The method according to claim 21, wherein said step b) comprises connecting a passive circuit component to said at least one selected output pin and generating said externally applied potential through said passive circuit component.

23. (new) The method according to claim 22, wherein said step b) further comprises connecting said passive circuit component between said at least one selected output pin and a reference potential.

24. (new) The method according to claim 22, wherein said passive circuit component comprises a resistor.

25. (new) The method according to claim 21, wherein said at least one selected output pin in said step b) and said at least one chosen output pin in said step e) both comprise the same output pin among said at least one signal output pin.

26. (new) The method according to claim 21, wherein said at least one signal output pin comprises plural signal output pins including a first output pin and a second output pin that is distinct and separate from said first output pin, said at least one selected output pin in said step b) is said first output pin, and said at least one chosen output pin in said step e) is said second output pin.

27. (new) The method according to claim 21,

further comprising varying said externally applied potential so that said potential value of said externally applied potential is initially a first potential value and is then a second potential value different from said first potential value,

wherein said at least one test signal generated in said step e) comprises plural test signals including a first test signal and a second test signal different from said first test signal; and

further comprising providing said first test signal to said chosen output pin dependent on and responsive to said evaluating in said step c) determining that said externally applied potential has said first potential value, and

providing said second test signal to said chosen output pin dependent on and responsive to said evaluating in said step c) determining that said externally applied potential has said second potential value.

28. (new) The method according to claim 27, wherein said circuit unit comprises plural circuit blocks including a first circuit block and a second circuit block, and further comprising activating said first circuit block and deactivating said second circuit block dependent on and responsive to said evaluating in said step c) determining that said externally applied potential has said first potential value, and activating said second circuit block and deactivating said first circuit block dependent on and responsive to said evaluating in said step c) determining that said externally applied potential has said second potential value.

29. (new) The method according to claim 21, wherein said circuit unit comprises plural circuit blocks, and further comprising respectively activating and deactivating different ones of said circuit blocks dependent on and responsive to a result of said evaluating.

30. (new) The method according to claim 21, wherein said steps d) and e) are carried out at a time separate from said steps b) and c), and not overlapping with said steps b) and c).

31. (new) The method according to claim 21, wherein said evaluating in said step c) comprises comparing said potential value to at least one reference value.

32. (new) The method according to claim 21, wherein said evaluating in said step c) comprises comparing said potential value to at least one reference value range defined by an upper reference value and a lower reference value, so as to determine whether said potential value falls in said reference value range.

33. (new) The method according to claim 21, wherein said evaluating in said step c) comprises performing a logical operation on said potential value and a signal value of said at least one output signal generated by said circuit unit.

34. (new) The method according to claim 33, wherein said step d) switches into said test mode only when said signal value is zero and said potential value lies in a prescribed potential value range.

35. (new) The method according to claim 21, wherein said evaluating in said step c) comprises determining whether said potential value lies within a voltage interval of a voltage window discriminator, and said step d) switches into said test mode only when said potential value does lie

within said voltage interval of said voltage window discriminator.

36. (new) The method according to claim 35, wherein a signal value of said at least one test signal also lies within said voltage interval of said voltage window discriminator.

[RESPONSE CONTINUES ON NEXT PAGE]